ECE2999: Independent Study

Line Counter Clock

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Advisor Signature: _____ _____

(Stephen J. Bitar) *(Date)*

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Abstract

The goal of this project was to create a working implementation of a line counter clock - a device that uses the 60Hz signal from wall power as a clock source to keep track of time. The idea of a mechanical clock that used a synchronous motor first came about at the 1893 Chicago World's fair by Nikola Tesla, although they were not implemented until some time later. With modern semiconductors, a digital clock can be made in a fairly straightforward fashion, using 60Hz as the timebase. I started this project in early 2022 to prove to myself that I could follow through with a somewhat complicated digital design. My original plan was to have LED's showing the current time in base 2, but I later added multiplexing circuitry to control seven segment displays. I also wanted to make the clock entirely using the 74xx family of logic chips, without any microcontrollers. Although this is certainly a little more challenging, as President Kennedy famously said, "We choose to do this not because it is easy, but because it is hard."

Acknowledgments

Thank you, Dave Crafts, for proposing the idea of this project and giving insights to possible revisions.

Introduction

The intention of this project is to count towards my undergraduate Electrical and Computer Engineering degree. One of the many lessons that I have learned through hands-on experience with electronics is that using the minimum number of wires / connections necessary is a plus. This clock uses its power source to keep track of time as well – 12VAC at 60Hz. This 60Hz is fairly precise as well: power companies will keep track of how many cycles have passed in a day and adjust the speed of turbines to ensure an average of 60.00 cycles per second. At its core, this project is a multi-stage / cascaded counter, with an appropriate clock speed. Each number of six total seven-segment LEDs have a corresponding decade counter. This document focuses on the design, operation, and PCB layout of this circuit.

Block Diagram

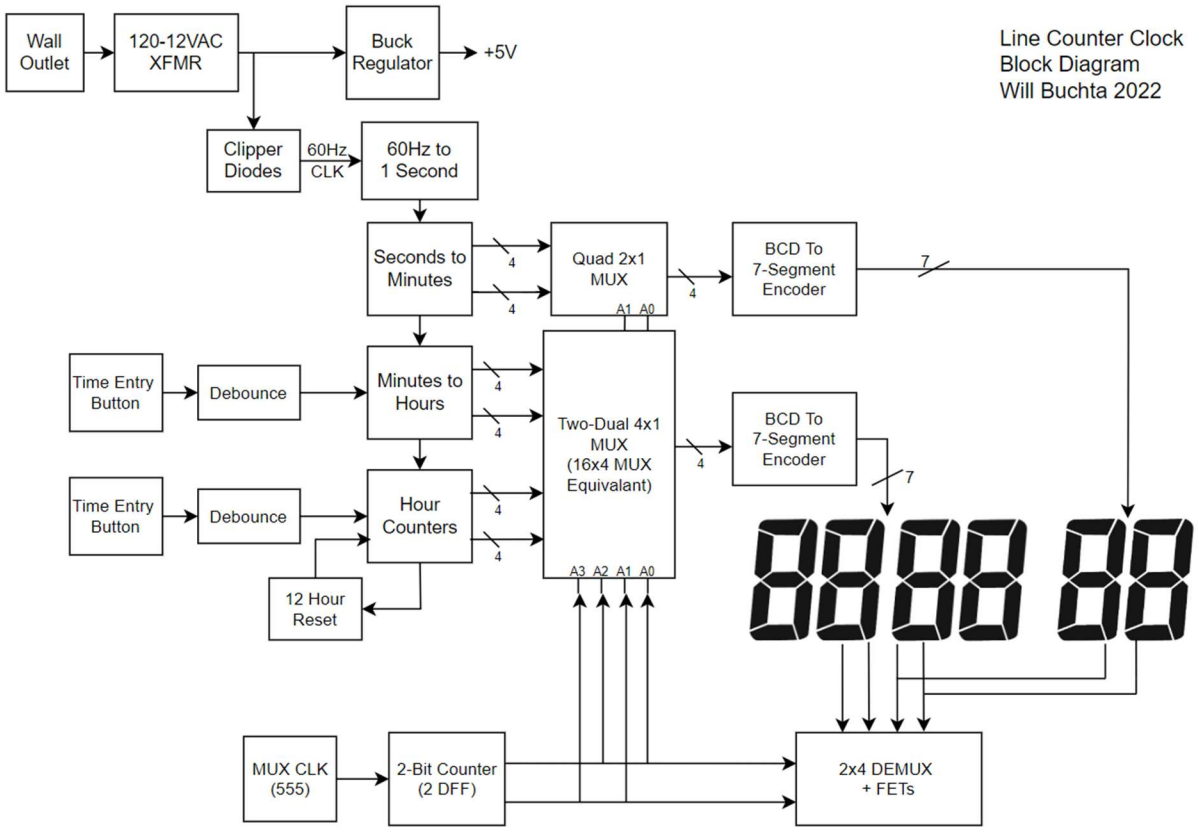

Figure 0: Block Diagram

Circuit Descriptions: Power Stage

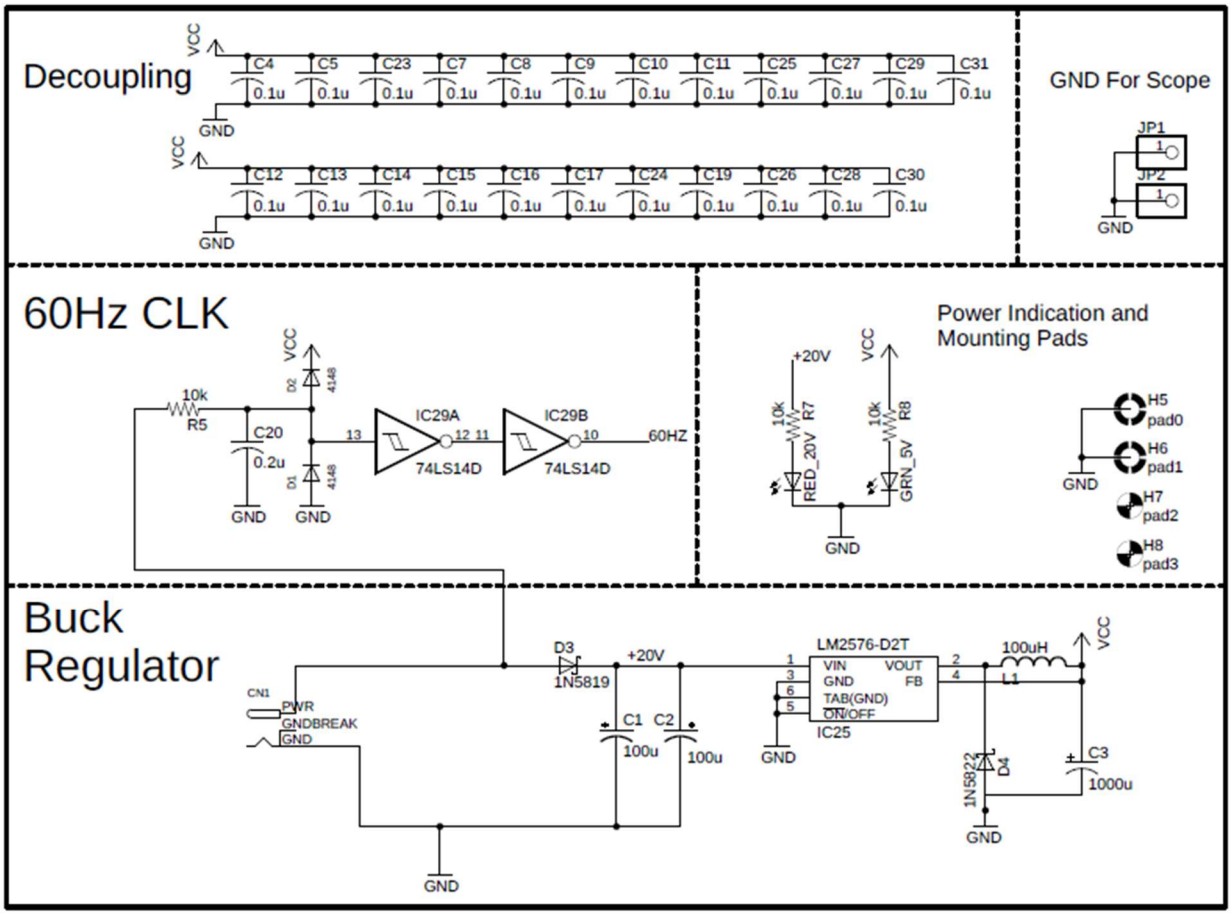

Figure 1: Power Delivery Schematic

Focusing first on power delivery, I chose to use a switching regulator to supply a 5V power rail – note that all chips are 5V tolerant. The AC from the wall is stepped through a half-wave rectifier (D3) and filtered with C1 and C2. This “lumpy” DC is fed into IC25, a buck converter. Linear regulators would not have sufficed due to the ~15 volts at load conditions they would need to dissipate. Note that although the wall transformer I bought is rated at 12VAC, it consistently outputs slightly over 14VAC. The schematic of this regulator was followed from the typical application in its datasheet. Note that it is rated for 3A of continuous draw, which is killing a fly with a sledgehammer as this board shouldn’t draw more than 50mA, but it is what I had on hand at the time. You can’t beat free.

Looking at the 60Hz clock section, one can see that I grabbed the AC waveform before the rectifier. I passed it through an RC lowpass filter with a bandwidth of around 80Hz in order to

eliminate any high frequency noise that may cause a false clock. This signal is then clipped from -0.7 to +5.7V before being fed into a Schmitt trigger inverter. The Schmitt trigger is necessary, as the rise / fall times are very slow in CMOS standards. Any noise on the signal could result in the input voltage fluctuating many times over and under the threshold voltage of a chip, causing multiple clocks. This is fixed with hysteresis. Upon review, it is apparent that IC29B is redundant and the 60Hz signal does not need to be inverted twice. Another improvement would be to add a high pass filter to form a bandpass, or cascading multiple filters to add poles.

I also have two LEDs indicating that the power supplies are good, both before and after the regulator. In the top right corner of Figure 1 is two pin headers that I have tied to ground, which is a trick of the trade to be used as an oscilloscope ground. Putting a loop of bare wire between the holes serves as an excellent probe clip. Although the ground may be far away from some signals that I might try to measure, there are no seriously high frequency components on this board. Shown as well are all the decoupling capacitors for the board. Looking back, I could have done a much better job of decoupling, which will be discussed later. On the design side (schematic) of things, I should have put each capacitor next to its respective IC, and added 1uF capacitors in parallel to achieve a broad spectrum of decoupling.

Power Stage Waveforms

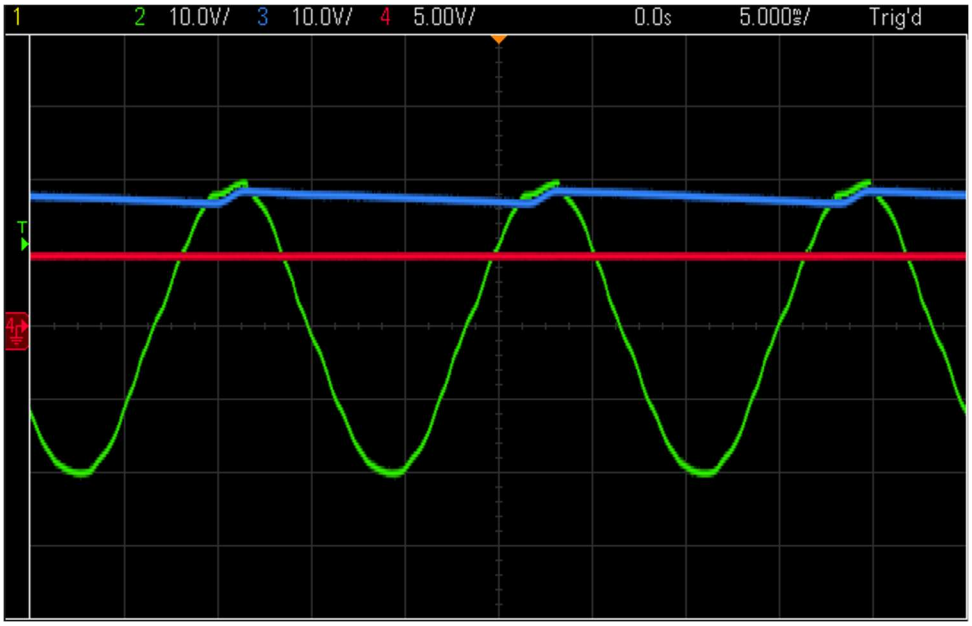

Figure 2: Stages of regulation

Shown above is an oscillogram of the stages of voltage regulation. Green is the $20V_{peak}$ input, blue is after the rectifier but before the regulator, and red is the regulated 5V output. The telltale dip in rectified voltage is seen in blue.

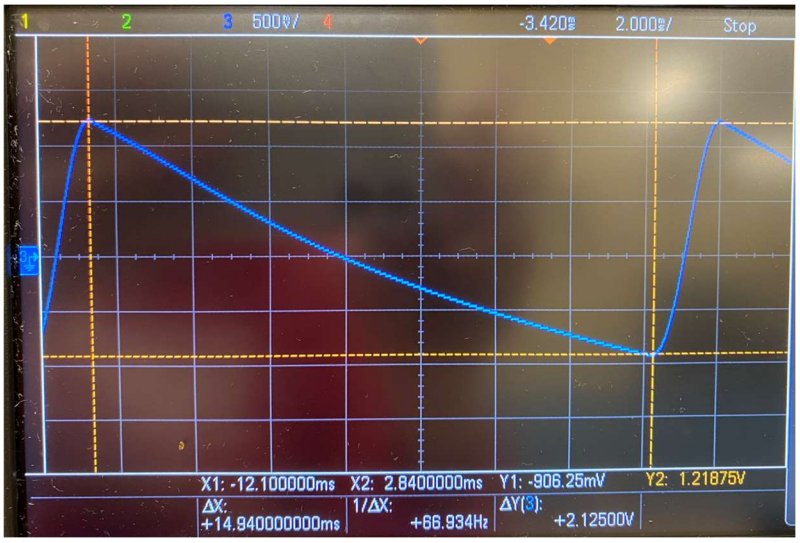

Figure 3: Input ripple

In Figure 3, the power supply ripple is seen with AC Coupling. Although the voltage and current on a capacitor is exponential in nature, the power draw of this board can be estimated linearly using $I = C\frac{dV}{dt}$. Plugging into a calculator with dV = 2.125V, dt =14.94ms, and C=200uF results in

approximately 28.4mA. Keep in mind that the capacitors are +/- 10% of their rated value. Current draw was measured later to be around 24mA. The majority of this current is consumed by the seven segment display.

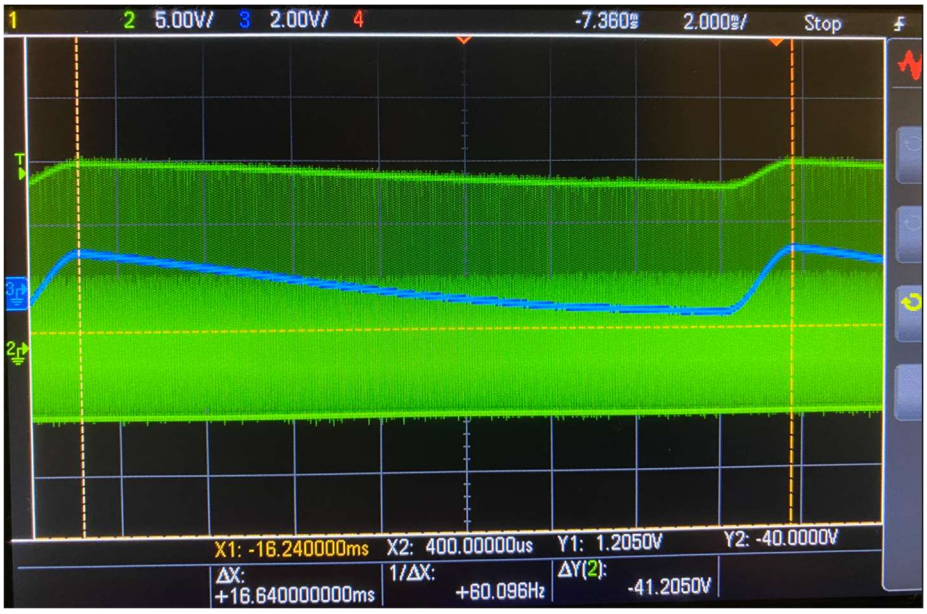

Figure 4: High frequency switching node of regulator

Figure 4 Above shows the output (Pin 2) of the buck regulator. Notice how the switch node high-level voltage dips in accordance with the input – a characteristic of Buck Regulators.

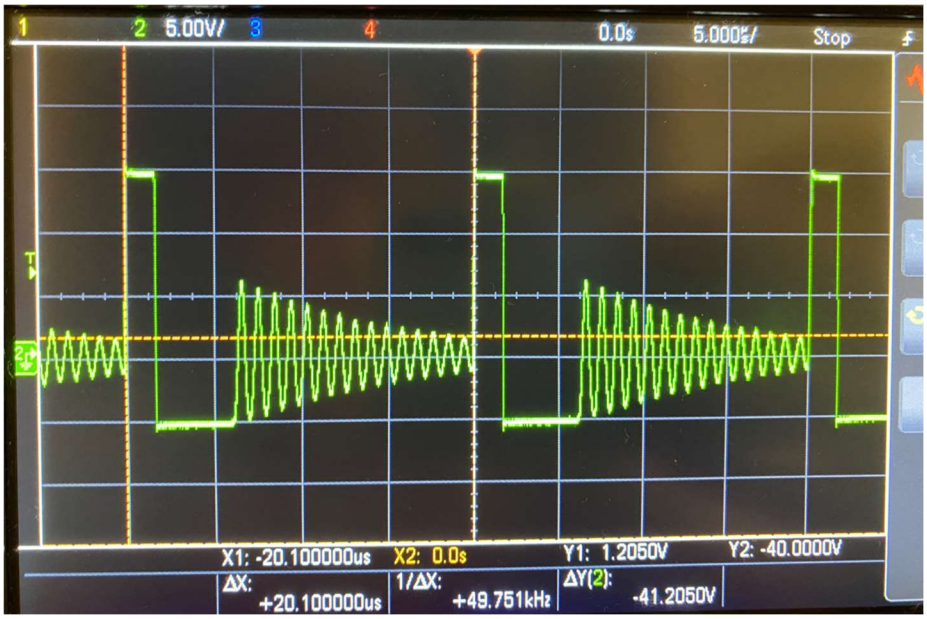

Figure 5: Zoomed in switching node

Zooming in further, we can see that there is an atrocious amount of ringing on the switch node, likely due to my imperfect layout. This will be discussed later. Note also the switching frequency of 49.7kHz, close to 52kHz specified in the datasheet.

Figure 6: DC-Rail noise

Shown above is the 5V rail with AC coupling. At the transitions of the switching node, there is a sharp spike of approximately 70mV. This noise would be unacceptable in an analog circuit, but as this is a purely digital board, I can get away with it. Essentially, I need more decoupling capacitors and a better layout around the regulator.

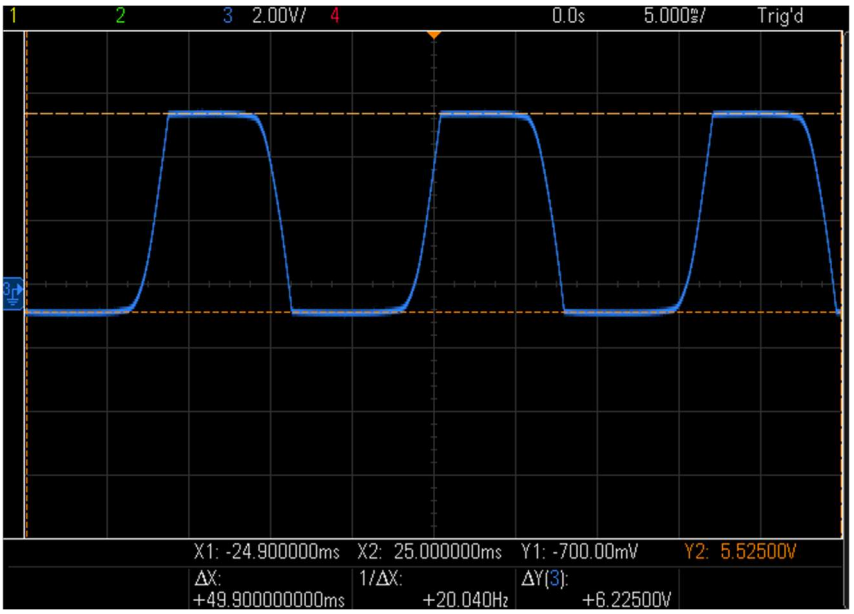

Figure 7: Clipped clock signal

Seen above is the input signal after clipper diodes. Note the signal going from -700mV to 5.53V, both near the characteristic forward voltage of silicon diodes.

Circuit Descriptions: Seconds and Minutes Counter

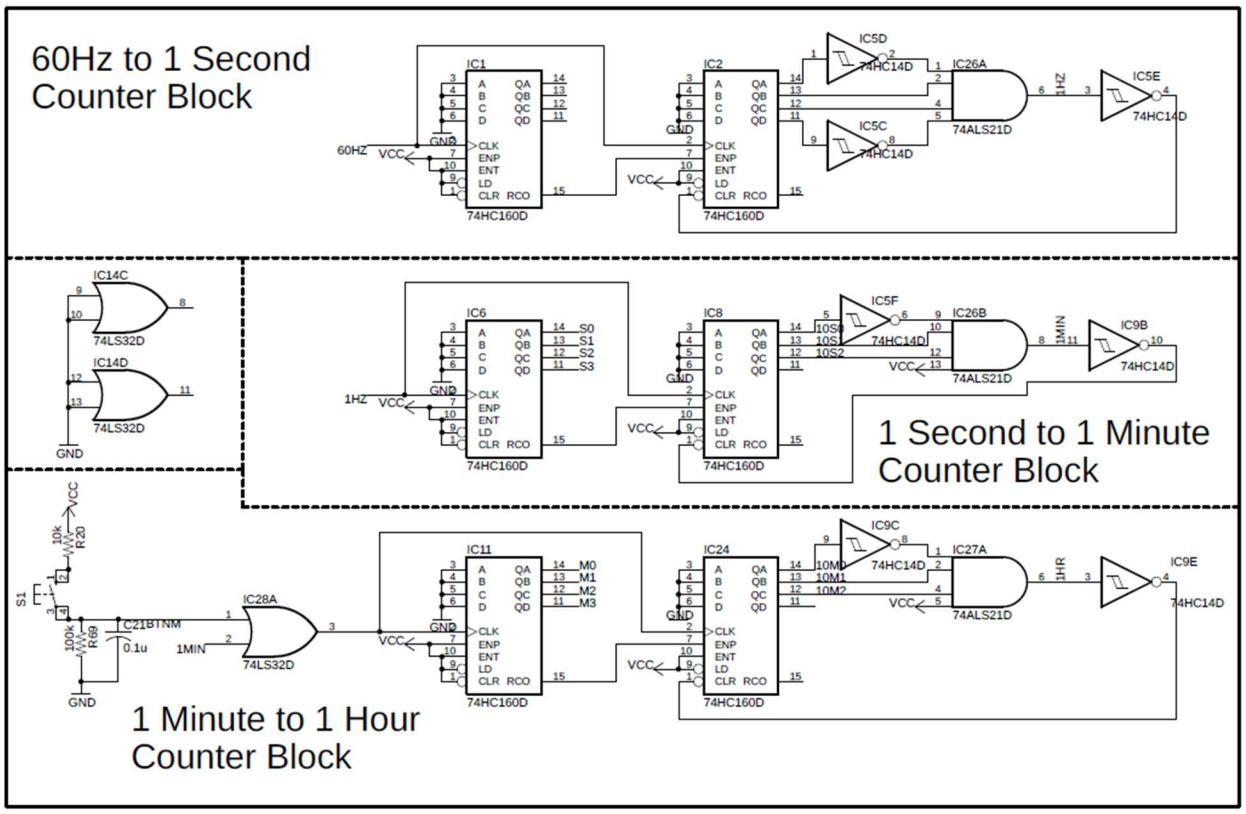

Figure 8: Seconds and Minutes counter blocks

Above are three identical counting blocks. Each block is composed of two decade counters (74xx160). The first counter goes from 0-9, and the second one from 0-5. Focusing on IC1, Ripple Carry Out (RCO) will go high when QA…QD = 1001, enabling IC2. On the next clock, IC1 will reset, and IC2 will increment by 1. As soon as IC2 reaches 6, the circuitry shown will reset the counter asynchronously. It also functions as the clock for the next stage. A drawback to this design is that the clock's pulse width will only be that of the propagation delays of the involved ICs – quite small (see Figure 9: pulse width is around 16ns). An improvement here would be to design a synchronous reset instead. IC5C is also redundant, since the counter will reset before QD will go high. In the seconds and minutes blocks, I tied the inputs to VCC. A clock would be rather useless if it can't be programmed, which is why I OR'd the clk signal to the minutes counters with a button. To eliminate bounce, I passed it through a low pass filter. In order for this to work however, the OR gate must have Schmitt trigger inputs to account for relatively slow input rise times as discussed earlier.

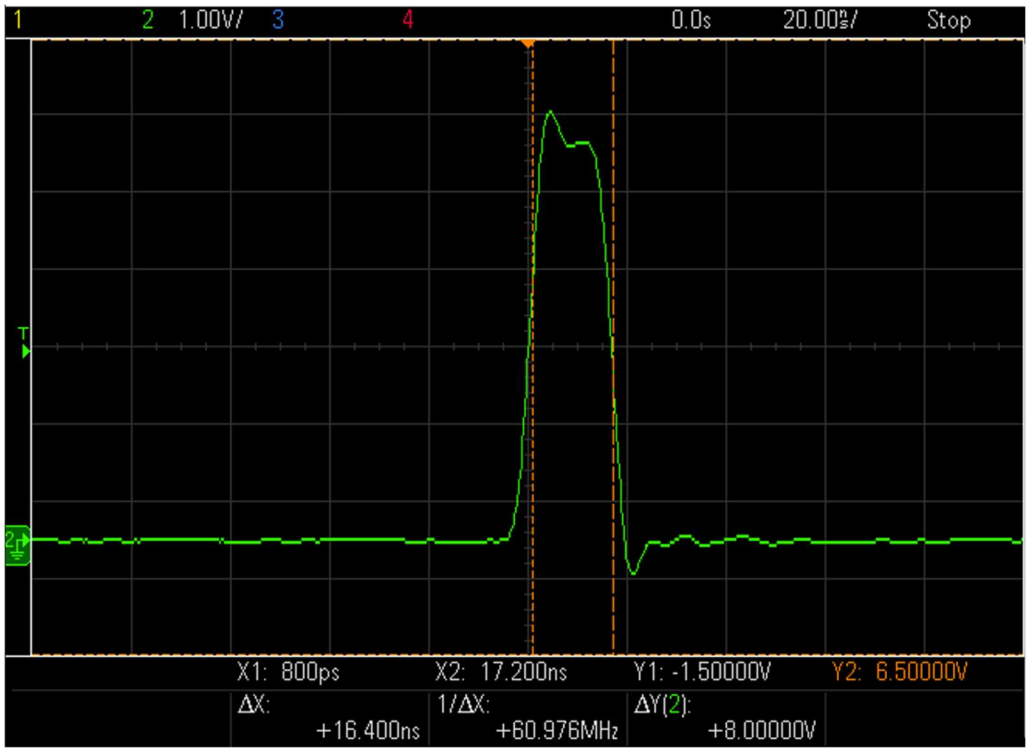

Figure 9: Reset Clock

Circuit Descriptions: Hour Counters

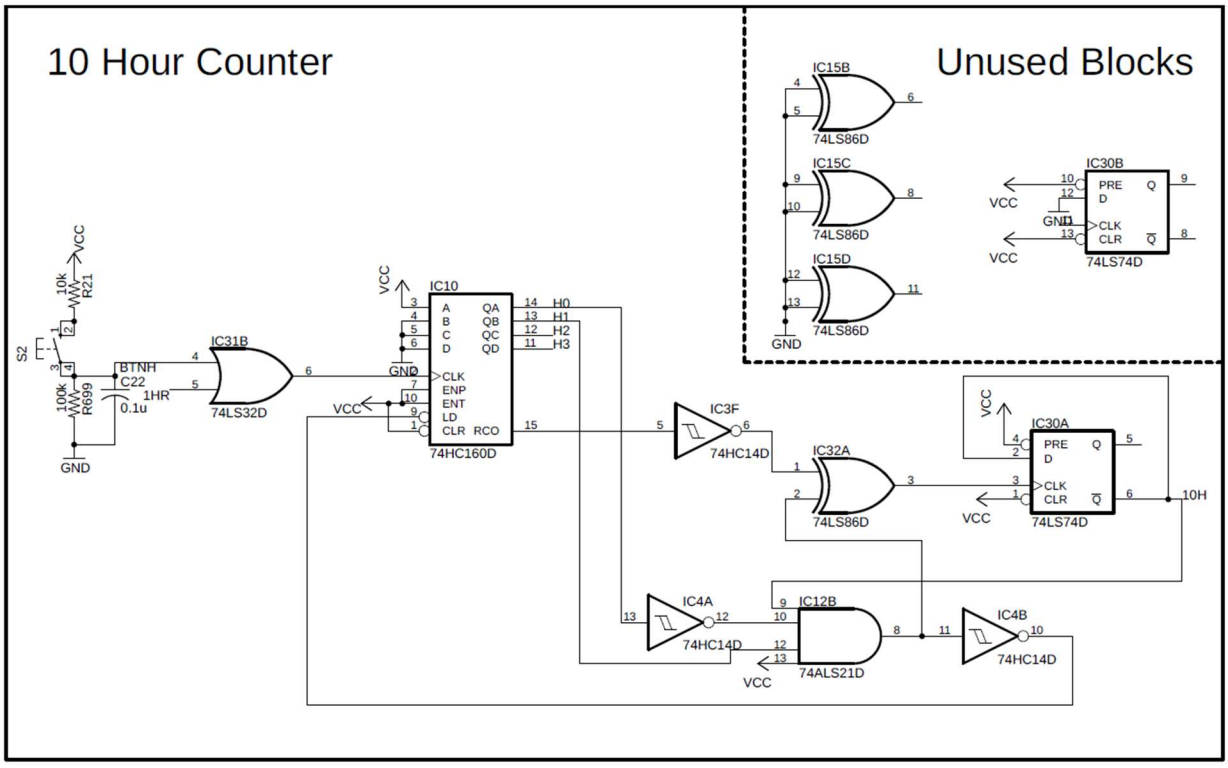

Figure 10: Keeping Track of Hours

Special logic was needed for the hours and tens of hours digits. Note the sequence of the hours: 01->02->03->04->05->06->07->08->09->1**0**->11->12->**01**. The one's digit needs to reset to 0 normally when the hours go from 9 to 10, and reset to 1 when the hours switch from 12 to 1. Since the ten's digit will only be 0 or 1, I chose to use a d flip flop to avoid using another 160 counter. Let's assume that the time starts initially at 08. At the next hour, IC10 reads 1001 on its output, and (R)ipple (C)arry (O)ut goes high, pulling the DFF's clock low. IC10 will then reset to 0000, putting RCO low, clocking the DFF. Since IC30A_Q was initially at 0 and Qnot at 1, IC30A_D is high, putting IC30A_Q high (when RCO goes low). Next, when IC10 hits 2 (0010), IC21B will go high, pulling the DFF's clock low (XOR logic), and IC10's LOAD pin low (the load pin is used to clock a specific value in the counter, similar to preset. It is also active low). With IC10 in load mode, it will put 0001 on its output at the next hour (after 12:59:59). This causes the AND gate to go low, clocking the DFF, and setting Qnot to 0. All of IC15's unused gates are tied low to keep it in a defined state.

Circuit Descriptions: Multiplexing

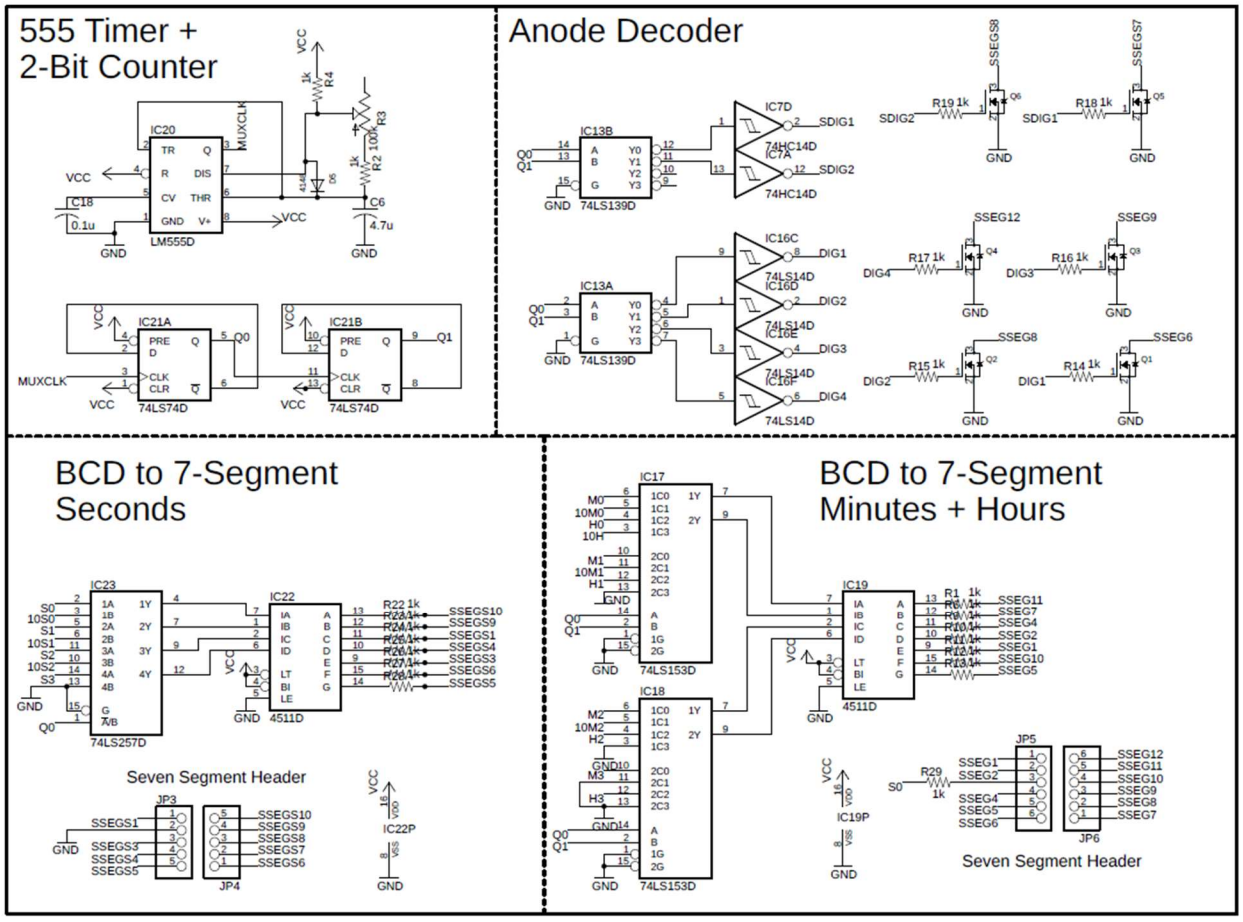

Figure 11: Multiplexing Circuitry

My original plan for this clock was to display the time in binary on several LEDs, but I decided that was going to be too simple. I was also going to use 74xx163 counters, which are synchronous reset 4-bit counters. Displaying seconds, minutes, and hours would be easy in binary by combining two 163's to form an 8-bit counter. However, binary is not easy to read, and clocks are only useful if you can tell what time it is. 7-Segment displays are much more visually appealing and give a retro look, but they do require special care. Using the 160 chips allows for easy storage of the time in binary coded decimal (BCD). The multiplexing circuitry above takes the BCD and connects the corresponding cathodes/anodes to power.

For the hours and minutes digits, I chose to use four 4x1 multiplexers in two 74xx153 chips. I tied their selector lines together to act as one 4-bit 4 to 1 mux. The output of the mux goes into a 4511 chip, which is a BCD to 7-segment display decoder. The same logic is repeated for the seconds digits, but I used a quad 2-1 mux configured as a 4-bit 2-1 MUX, as I only needed to control two digits. The select lines are controlled via a 2-bit counter made from D Flip Flops,

which is clocked by an adjustable 555 timer (see operation in Figure 12. Note that the output changes state as the capacitor reaches 1/3 and 2/3 of Vdd). I added a 100k potentiometer in series with the timing capacitor's discharge route, which can slow down the multiplexing enough to see each individual digit flash. Since the displays are common cathode, I used 2-4 bit decoders to control each digit's cathode, taking care to make sure that the correct digit would be "on" at the right time with the corresponding counter data. Note that SDIG1(seconds digit 1) and SDIG as well as SGID2 and DIG2 are the same signals; I overlooked this in the design, and they could be tied together. I chose to use a 2-bit decoder for the seconds digits' anodes rather than 1 bit, to make sure all displays would be the same brightness. The minutes and hours have a duty cycle of 25%, so if I used a 1 bit counter, the seconds digits would be twice as bright.

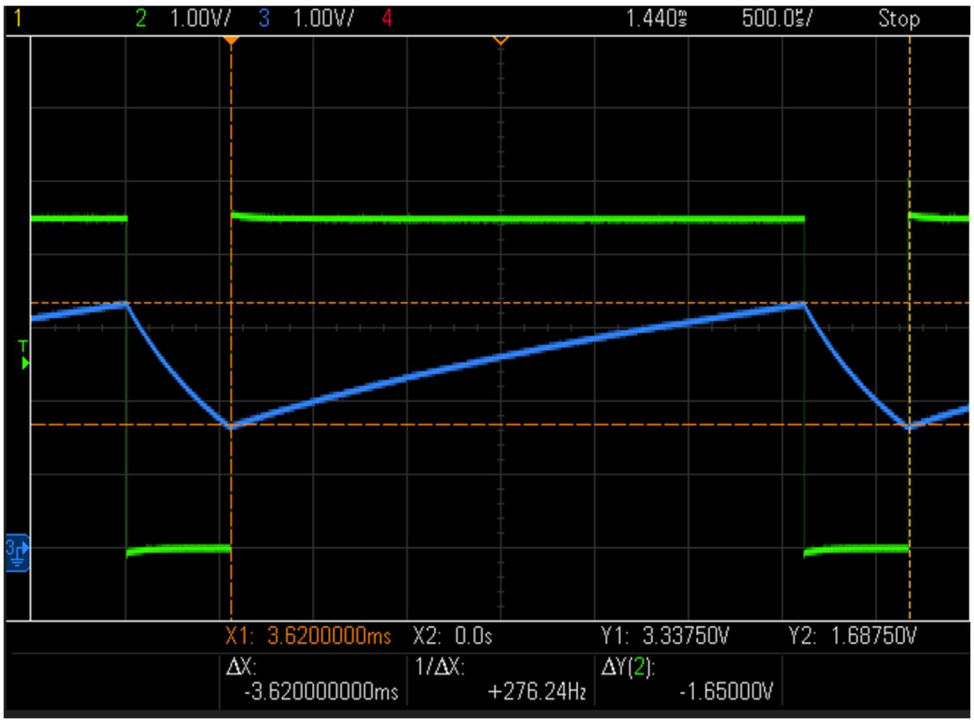

Figure 12: 555 Timer Operation

Layout

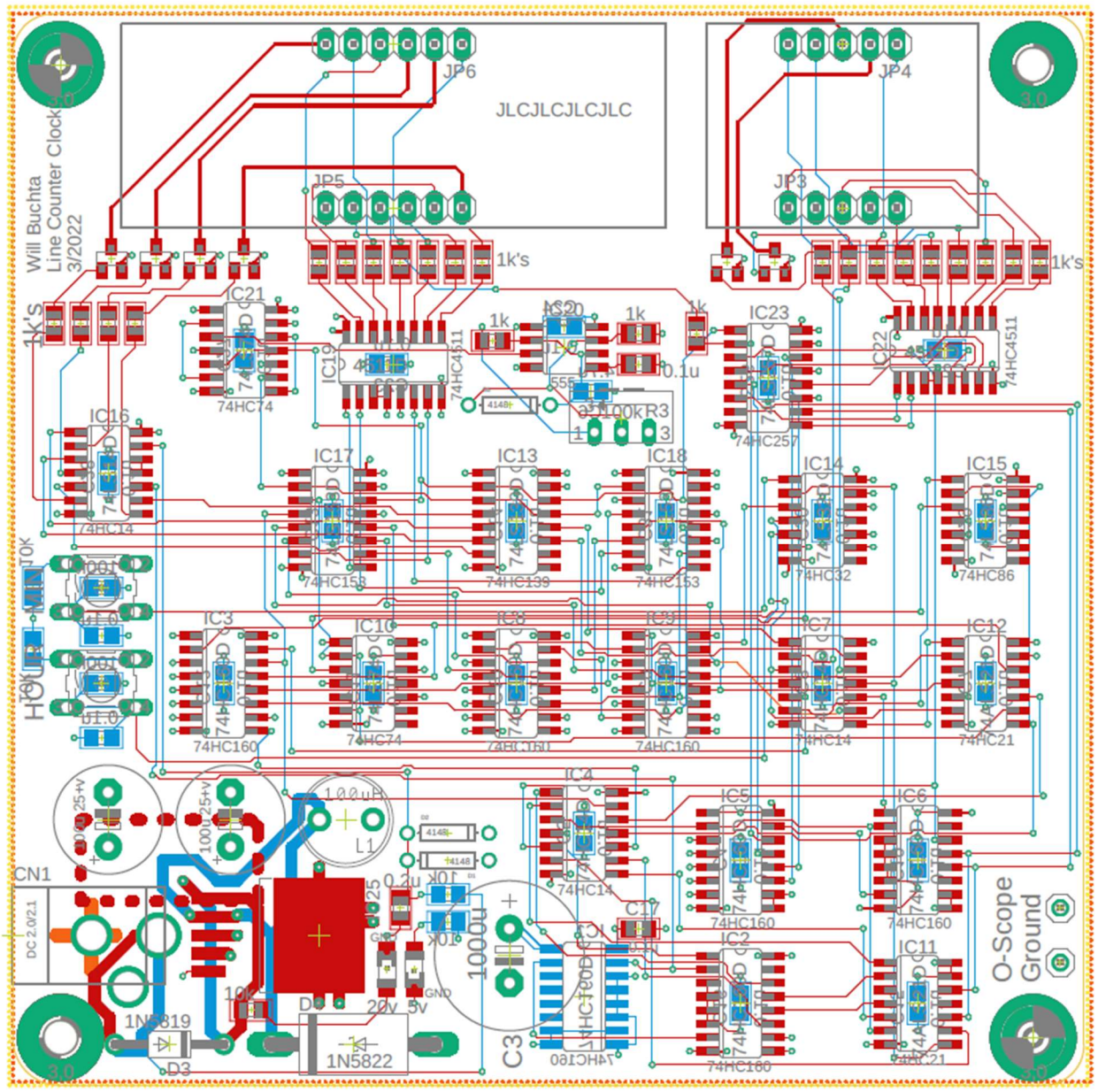

Figure 13: PCB Layout

Above is the layout of the printed circuit board. The stack up is as follows: Signal - PWR – GND – Signal. I followed a general up/down on the bottom layer and left/right on the top to aid in routing. There are several improvements that I can make here, starting with decoupling.

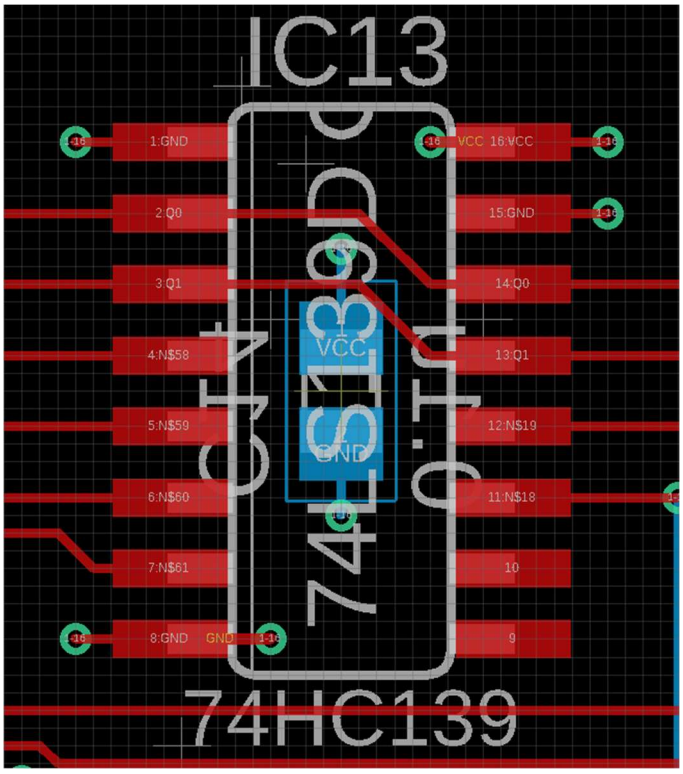

Figure 14: Decoupling for each IC

Power supply decoupling is useful to mitigate high frequency noise that may be present. The above screenshot shows the decoupling for each chip on the board. I mounted capacitors directly underneath each IC, with vias to power and ground planes. This results in poor decoupling; note the long, thin traces connecting to small vias, resulting in large inductances between the power pins and the caps. I also only used one value capacitor for decoupling, which fails to eliminate a wide spectrum of noise. An improved layout is shown below.

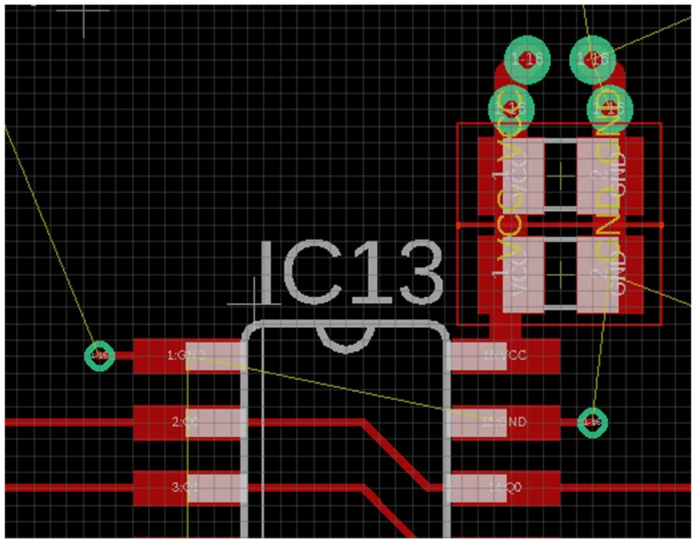

Figure 15: Improved Decoupling

Figure 15 shows an improved layout for decoupling. Focusing on the top right, we see that the power and ground vias are placed very close to each other to minimize stray inductance for a current-return path. Notice how current must flow through the capacitors before it reaches the chip. The cap closest to the power pin is a 0.1uF, and further is a 1uF.

At high frequencies, the return current for any signal is directly underneath the corresponding trace. If the signal passes through a via, it changes reference planes, which is why it is necessary to drop a ground via for each signal via. I did not use this practice in the layout, which is a possible further improvement.

During assembly and debugging of the board, I noticed that it was challenging to scope various signals. Another improvement to this board would be to add test points on more important traces.

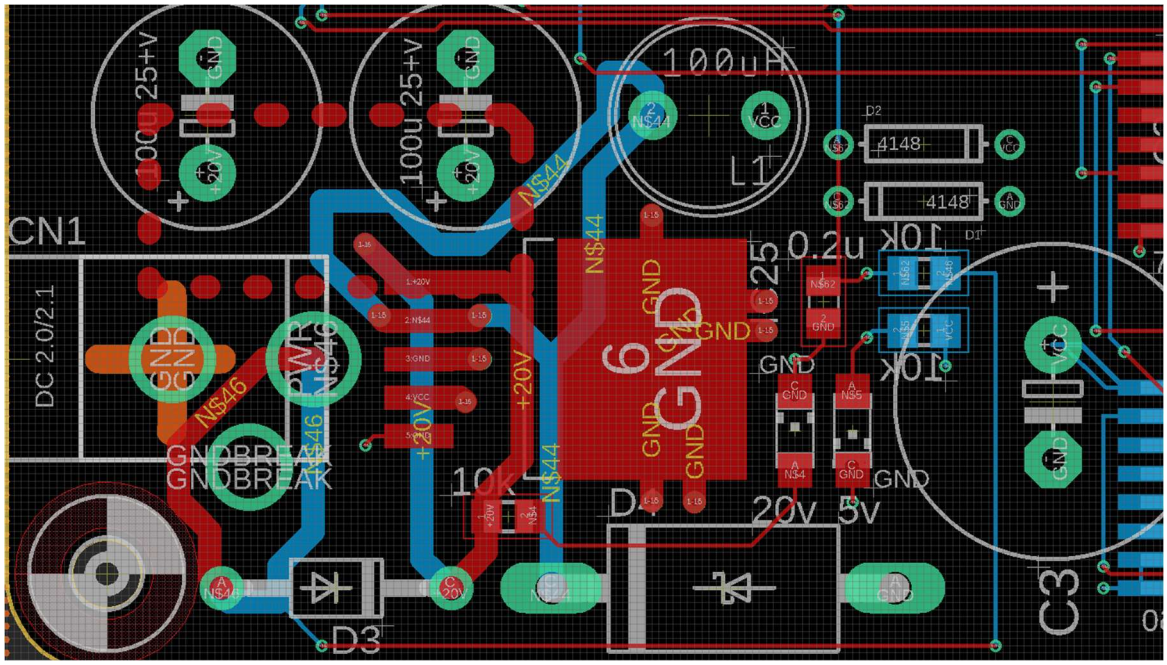

Figure 16: Buck Regulator Layout

Shown above is the layout of the power stage. This layout resulted in lots of ringing, as discussed earlier and in Figure 6. I do not have enough ground vias here, and connections on the switching node switch layers without a ground via. To improve this, I should route all related signals on the same layer with the same reference plane. I can also use copper pours to minimize stray inductance. Additionally, I can rearrange things to make the layout generally tighter. This is discussed in *much* more depth in the cited application notes / videos.

References

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